UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/673,626	09/29/2003	Jungwon Suh	2003P52600US (I331.112.10	2545

7590 11/07/2005

EXAMINER	
KO, DANIEL BOKMIN	

ART UNIT	PAPER NUMBER
2189	

Dicke, Billig & Czaja, PLLC
Fifth Street Towers
Suite 2250
100 South Fifth Street
Minneapolis, MN 55402

DATE MAILED: 11/07/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/673,626	SUH, JUNGWON	
	Examiner	Art Unit	
	Daniel B. Ko	2189	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *18* is/are allowed.

6)☒ Claim(s) *1-3,5-9,11-15 and 17* is/are rejected.

7)☐ Claim(s) *4,10 and 16* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *9/29/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This action is responsive to the application filed on 9/29/2003. Claims 1-18 have been submitted for examination.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

1. Claim 1 rejected under 35 U.S.C. 102(e) as being anticipated by Keeth et al. (US Patent 6,807,114 B2), hereinafter simply Keeth.

Keeth teaches as claimed including a fuse banks for programming respective addresses to defective columns and a defective column decoder that determines which way column select signals should go (See abstract).

Regarding claim 1, Keeth teaches a dynamic random access memory device capable of converting from a full density memory device to a reduced density memory

device to compensate for cell failures in a plurality of cell blocks, the memory device comprising:

a row address mapping fuse (Fig. 1, element 51, fuse bank) for selectively determining row address combinations void of cell failures and capable of storing data bits (column 4, lines 40-61); and

row address mapping logic (Fig. 2, element 52, column select circuit) coupled to the row address mapping fuse for receiving a row address mapping signal from the row address mapping fuse and receiving row address signals and or routing specific data bits to the row address combinations void of cell failures and capable of storing the data bits (column 5, lines 62-67, column 6, lines 1-58).

Keeth's description teaches mainly for defective column replacement but it discloses that the system and method can also be used to replace defective rows of memory cells in the substantially the same manner (column 2, lines 61-63).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

2. Claims 2-3, 5-9, 11-15, and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Keeth (US Patent 6,807,114 B2) and Cowles et al. (US Patent 6,556,497 B2), hereinafter simply Cowles.

Regarding claim 2, Keeth teaches a dynamic random access memory device comprising:

a logic value setting signal;

a multiplexer having a first input coupled to the reduced density enable signal, a second input coupled to the logic value setting signal, and a third input coupled to a row address (Fig. 2, element 18, row-address MUX; column 4, lines 12-28);

wherein an output signal of the multiplexer is coupled to an input of the row address mapping logic; and

a logic value setting signal.

Applicant's a logic value setting signal together with a row address mapping fuse and an output signal of the multiplexer routes data to the valid address void of cell

failures. Keeth discloses the column select circuit that redirects the defective column memory cells to next lower or higher numbered column so that data can be routes to valid address void of cell failure (column 5, lines 62-67; column 6, lines 1-32).

Keeth fails to teach a switching the memory device between a full density mode and a reduced density node. Cowles teaches a dual mode, full density/half density SDRAM (See abstract).

Cowles teaches a reduced density enable signal for switching the memory device between a full density mode and a reduced density mode (column 4, lines 31-61).

At the time of invention it would have been obvious to a person of ordinary skill in the art to combine the Keeth with Cowles. The motivation for doing so would have been a flexibility of density mode. The DRAM can be used as a full density mode or a half density mode based on user's need.

Regarding claim 3, Keeth teaches a dynamic random access memory device, wherein the row address mapping logic receives a plurality of row address signals from a row address multiplexer and the output signal of the multiplexer (column 4, lines 12-28). It is obvious that the row address MUX (Keeth, element 18) can be connected to column select circuit 52 and receives a plurality of row address signals.

Regarding claim 5, Keeth teaches a dynamic random access memory, wherein the output signal of the multiplexer is the row address when the memory device is operating in the full density mode (column 4, lines 12-28).

Regarding claim 6, Keeth teaches a dynamic random access memory, and further comprising:

a plurality of row address mapping fuses (Fig. 2, elements 51, fuse bank; two fuse bank disclosed);

a plurality of row address mapping logics (Fig. 2, elements 52, column select steering circuit; two column select steering circuits disclosed);

a plurality of bank cell arrays (Fig. 2, elements 20 and 22, bank 0 memory array and bank 1 memory array; two bank memory array disclosed); and

wherein an output of each row address mapping logic is coupled to a corresponding input of a bank cell array such that data bits may be routed to row address combinations void of cell failures and capable of storing the data bits within the particular bank cell array independent of other bank cell arrays (column 6, lines 9-32).

Regarding claims 7 and 17, Keeth teaches a dynamic random access memory, wherein the row address mapping logic utilizes a selection table defining selected locations void of cell failures and capable of storing the data bits (column 5, lines 19-30). Keeth discloses the defective column of memory cell and it is obvious that a selection table can be made defining selected locations void of cell failure.

Regarding claims 8 and 14, Keeth teaches a method of converting a full density memory device to a reduced density memory device, the method comprising:

selectively determining a reduced density address combination having addresses which omit cell blocks having cell block failures (column 5, lines 19-61); and

storing data bits at an address (column 6, lines 9-15) within the reduced density (See Cowles, column 4, lines 31-61) column address combination.

Regarding claims 9 and 15, Cowles teaches a method of claim 8, and further comprising:

switching the memory device between a full density mode and a reduced density mode (column 4, lines 31-61).

Regarding claims 11 and 12, Keeth teaches a method, wherein the step of selectively determining a reduced density address combination further comprises:

selectively determining a plurality of addresses which avoid cell blocks having cell block failures (column 5, lines 19-61).

Regarding claim 13, Keeth teaches a method, wherein the step of selectively determining a reduced density address combination further comprises:

selectively determining a reduced density address combination based upon a row address mapping signal in combination with a logic value signal (column 5, lines 62-67, column 6, lines 1-58).

Allowable Subject Matter

3. Claim 18 is allowed.

4. Claims 4, 10, and 16 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Daniel B. Ko whose telephone number is 571-272-8194.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Manorama Padmanabhan can be reached on 571-272-4210. The fax phone number for the organization where this application or proceeding is assigned is 703-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Daniel B. Ko
AU 2189

KEVIN VERBRUGGE
PRIMARY EXAMINER